(12) **EUROPEAN PATENT SPECIFICATION**

(54) **Imaging coding device and method**

Einrichtung und Verfahren zur Bildkodierung

Dispositif et procédé pour le codage d'images

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Description

The present invention relates to an image coding device and method for compression coding of image data, and more particularly, to an image coding device and method for coding image data by means of an arithmetic code.

As described in ISO/IEC (Committee Draft 11544, etc.), an arithmetic code is used for image encoding by adaptive prediction or the like.

An example of the construction of a coding circuit using the arithmetic code is illustrated in Fig. 1.

Binary data I of a target picture-element to be coded is input to an exclusive-OR gate 904. Binary data X_0 to X_n of a plurality of reference picture-elements adjacent to the target picture-element is input to a predictive-state memory 901. The predictive-state memory 901 inputs 0 or 1 as predictive picture-element data to the exclusive-OR gate 904 in accordance with the state of the reference picture-elements data. In the exclusive-OR gate 904, examination of match/mismatch between the target picture-element data I and the predictive picture-element data from the predictive-state memory 901 is conducted, and the result of the examination is output to an arithmetic coding device 903.

The arithmetic coding device 903 is provided with an interval-size register (A-register) representing a current coding-interval and a code register (C-register), both of which are shifted in accordance with the output value of the exclusive-OR gate 904. Subsequently, a consecutive 8-bit value at a specific position in the C-register is output as code data.

The content of the predictive-state memory 901 is updated in accordance with the direction of the predictive-state updating part 902 which fetches the coded result including the value of the A-register in the arithmetic coding device 903. Consequently, the predictive picture-element data is output to the exclusive-OR gate 904 from the predictive-state memory 901 adaptively to the coding operation being executed.

Fig. 2A is a flow chart showing the coding operation of the coding device 903. Let the A-register be 32 bits and the C-register also be 32 bits in the coding device 903. By definition, the interval A ranges between 0 (0000H) and 0.5(8000H) and 1.0(10000H), where H represents a hexadecimal integer.

After the comparison between data of the target picture-element and data of the predictive picture-element by the exclusive-OR gate 904, a constant LSZ (least significant coding interval) is subtracted (S 201) from the value A of the A-register in the arithmetic coding device 903. The constant LSZ corresponds to the occurrence probability of a less probable symbol. Subsequently, the match/mismatch between the target picture-element and the predictive picture-element is determined (S202) in the exclusive-OR gate 904. When a match occurs, re-normalization as shown in Fig. 3 is executed. On the other hand, another re-normalization as shown in Fig. 4

is executed when a mismatch occurs. The re-normalization procedure is illustrated in Fig. 2A, in which re-normalization can be executed either when a mismatch between the target picture-element data and the predictive picture-element data occurs, or when a match between the two data occurs and the value A of the A-register is less than 0.5(8000H).

As shown in Fig. 2B, to double the respective contents of the A-register and the C-register, these registers are respectively shifted to MSB by 1 bit each, and then 1 is subtracted (S301) from a CT-counter which counts the number of shifts. In this example, to treat the code data as 8-bit parallel data, the data at a specific position in the C-register is fetched as the code data whenever the C-register has shifted 8 times. Therefore, the 8-bit code data is obtained when "8" is initially set at the CT-counter; subtraction from the set value of the CT-counter is made at every 1-bit shift of the A-register; and the value of the CT-counter becomes "0."

Accordingly, a determination (S302) is made whether the value of the CT-counter is "0" or not, in which the 8-bit code data is fetched from the C-register and output (S303) the data when the value is "0"; although outputting of the code data is not executed when the value is not "0." Subsequently, it is determined (S304) whether the 1-bit shift value A of the A-register is less than 0.5 (8000H) or not. If the value A is 0.5 (8000H) or more, this re-normalization ends; and if it is less than 0.5 (8000H), the aforementioned shift operation is repeated by returning to the step S301 to execute each 1-bit shift of the A-register and the C-register and the 1-subtraction of the CT-counter. This shift operation is executed until the value of the A-register becomes 0.5 (8000H) or more.

A description of a state transition of the A-register in the re-normalization processing will now be given in conjunction with the examples shown in Figs. 3 and 4. When a match between the target picture-element data and the predictive picture-element data occurs, it is determined (S203) whether the value A of the A-register is less than 0.5 (8000H) or not. When the value A is 0.5 (8000H) or more, the coding operation ends through path 2 (as shown in Fig. 2A and phase 1 and phase 2 of Fig. 3). On the other hand, when the value A of the A-register is less than 0.5 (8000H), the A-register is updated (S204) by conducting a shift operation through path 1 so as to set the value A at 0.5 (8000H) or higher. The same shift operation is also executed (S205) for the C-register. Accordingly, updating of the A-register and the C-register can be executed (as shown in phase 3 of Fig. 3), in which the value of the CT-counter which counts the number of shifts of the A-register becomes "0" and consequently a high-order byte of the C-register is output as the code data.

When a mismatch occurs between the target picture-element data and the predictive picture-element data, the shift operation of the A-register will be executed until the value A of the A-register becomes 0.5

(8000H) or more (as shown in phases 1, 2, 3, and 4 in Fig. 4). As shown in Fig. 4, the shift operation of the A-register is executed three times. This shift operation accomplishes the updating (S206) of the A-register. The same shift operation is also executed (S207) for the C-register. As shown in Fig. 4, the value of the CT-counter becomes "0" at the first shift, and consequently the high-order byte of the C-register is output as code data. After the output, the value of the CT-counter is set at "8".

Accordingly, in the coding device 903, the re-normalization accompanied by the shift operation of the A-register and the C-register for the coding operation of each target picture-element is executed. The number of shifts for the re-normalization is determined by the match/mismatch between the target picture-element data and the predictive picture-element data, and by the value A of the A-register. The number of shifts is 1 when the value A is within the range of 4000H≤A≤7FFF, and 15 when A=0001H. Therefore, the required period for the re-normalization is not constant, which is not suitable for synchronous coding in real time with the inputting of the target picture-element to be coded.

US-A-4,286,256 discloses a method and apparatus for arithmetic coding utilising a reduced number of operations. The reduction is attained by constraining the values of the conditional binary probabilities to certain values. This enables each encoding cycle to be achieved with a single shift and subtract operation. This constraint has the effect that when a binary symbol corresponds to the least probable symbol, the register for storing interval data need not be updated during an encoding cycle.

An object of the present invention is to provide a coding device capable of high-speed coding operation in accordance with the arithmetic code.

The present invention provides an image coding device for coding image data by using an arithmetic code, comprising:

> examination means for examining coincidence/ noncoincidence between actual image data of a target pixel to be coded and predictive image data predicted with reference to image data of reference pixels adjacent to the target pixel;
> first register means for storing a plurality of bits of interval data to be used for coding the image data in accordance with an examination result from said examination means;
> second register means for storing a plurality of bits of code data in accordance with an examination result from said examination means;
> monitor means for monitoring plural bits of the interval data stored in said second register means in accordance with a monitoring result from said monitoring means, said shift means being adapted to shift the interval data and the code data by a plurality of bits at one time;
> holding means for holding an amount of shifts of the

code data executed by said shift means; and
> output control means for controlling the output of the code data from said second register means in accordance with the amount of shifts being held by said holding means and an amount of shifts of the code data executed by said shift means.

The present invention further provides an image coding method of coding image data by using an arithmetic code, comprising:

> an examining step of examining coincidence/non-coincidence between actual image data of a target pixel to be coded and predictive image data predicted with reference to image data of reference pixels adjacent to the target pixel;
> a first storing step of storing a plurality of bits of interval data to be used for coding the image data in a first register in accordance with an examination result of the examining step;
> a second storing step of storing a plurality of bits of code data in a second register in accordance with an examination result of the examining step;
> a monitoring step of monitoring plural bits of the interval data stored in the first register;
> a shifting step of shifting the interval data stored in the first register and the code data stored in the second register in accordance with a monitoring result of the monitoring step, the interval data and the code data being shifted by a plurality of bits at one time;
> a holding step of holding an amount of shifts of the code data in the first register; and
> a controlling step of controlling an output of the code data from the second register in accordance with the amount of shifts being held and an amount of shifts of the code data.

Other features and advantages of the present invention will become more apparent from the following description of the preferred embodiment taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating a coding circuit using an arithmetic code.

Fig. 2A is a flow chart showing a coding operation;

Fig. 2B is a flow chart showing re-normalization processing.

Fig. 3 is a schematic illustration showing a re-normalization operation when predictive match occurs.

Fig. 4 is a schematic illustration showing a re-normalization operation when predictive mismatch occurs.

Fig. 5 is a block diagram of a coding device according to the present invention.

Fig. 6 is a block circuit diagram of a priority encoder.

Fig. 7 is a table representing the relationship be-

tween the A-register and the number of shifts.

Fig. 8 is a table representing the correlation between the number of shifts and CT values.

Fig. 9 is a schematic diagram showing a construction of a barrel shifter.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A detailed description of the preferred embodiment of the present invention will now be given.

Fig. 5 is a construction diagram of a coding device to which the present invention is applied. The coding device shown in Fig. 5 is used in a coding device 903 shown in Fig. 1 to construct an image coding device using an arithmetic code. In Fig. 5, reference numeral 201 represents a C-register of 16 bits. Another numeral 202 represents an A-register of 16 bits, which stores data indicating current coding interval--one of the parameters to be used for coding image data. Reference numerals 203 and 204 represent barrel shifters for bit shifts of the C-register 201 and A-register 202 respectively. A numeral 205 represents a CT-register to hold a CT value. As shown in Fig. 2B, the CT-register conducts a subtracting operation by using a counter. However, in the embodiment according to the present invention, a register for simply holding an input CT-value is used.

A priority encoder 206 receives the outputs of the A-register 202 and the CT-register 205 as inputs to the encoder 206, then controls the amount of shifts of the barrel shifters 203 and 204, and updates the value of the CT-register 205 by controlling a CT update-logic 211. Furthermore, the priority encoder 206 controls a high-byte register 207 and low-byte register 208 to conduct an output control of each 1 byte of high-order position and low-order position of the data stored in the C-register 201. Still another reference numeral 209 is a carry-control circuit which is specific to the arithmetic code.

In a subtracter 212, LPZ generated by a LPZ generator 213 is subtracted from the value of the A-register 202, and consequently the subtracted result is input to the selector 214. Another input to the selector 214 is LPZ, which is directly provided to the selector 214 from the LPZ generator 213. The selector 214 selects one of the above-mentioned two inputs in accordance with the output of an exclusive-OR gate 904 which represents match/mismatch between a target picture-element and a predictive picture-element. Accordingly, when a match occurs between the target picture-element and the predictive picture-element, the selector 214 selects the output (A-LPZ) of the subtracter 212; and when mismatch takes place, the selector 214 selects the LPZ generated by the LPZ generator 213. Subsequently, the value A-LPZ or the value LPZ is input to the A-register 202, and then the value of the A-register 202 is updated.

On the other hand, in an adder 215, the value of the C-register 201 is added to the output (A-LPZ) of the subtracter 212, and consequently the addition result is input

to a gate 216. Subsequently, the gate 216 inputs the output of the adder 215 to the C-register 201 in accordance with the output of the exclusive-OR gate 904 which represents mismatch between the target picture-element and the predictive picture-element, thus enabling the updating of the value of the C-register 201.

Meanwhile, the value A of the A-register during the execution of re-normalization is $1 \leq A \leq 7FFFH$. Therefore, the number of bits which shift in accordance with the range of each A value can be uniformly defined. This results in "finding the bit positions closest to MSB among respective bit-positions storing the value 1 in the A-register 202." Accordingly, detection of the above-mentioned bit position is enabled by constructing a priority encoder 206 as shown in Fig. 6.

As shown in Fig. 6, the priority encoder 206 shown in Fig. 6 consists of a logical-circuit part 309 and a $16 \rightarrow 4$ encoder 308. Each storage bit of the A-register 202 is fetched by each parallel bit and is input to the logical-circuit part 309 which comprises inverters 302, 304, 306, ... and AND-gates 303, 305, 307, ... The logical-circuit part 309 is constructed in a manner such that AND gates 303, 305, 307, ..., which correspond with the bit positions closest to MSB among respective bit-positions storing the value 1 in the A-register 202, can only execute a high-level output. For example, when data such as "0101..." is stored in the A-register 202, the AND gate 303 which corresponds to the second-bit output MSB-1 in the A-register 202 can execute only the high-level output. The output of each AND-gate 303, 305, 307,... is input to the 16->4 encoder 308, and then 4-bit data which represents the bit position is output from the encoder 308.

Fig. 7 shows the association between the value of the A-register at the re-normalization and the number of shifts of the A-register 202. The number of shifts from the priority encoder 206 is input to barrel shifters 203 and 204 which consequently execute the shift of the contents of the C-register 201 and the A-register 202 by 1- to 15-bit shifts at one time in accordance with the number of shifts.

In Fig. 9, the construction of the barrel shifter 204 and the A-register 202 is shown. The construction of the barrel shifter 203 and the C-register 201 is the same as this.

The 16-bit data stored in the A-register 202 is input to the barrel shifter 204 in parallel. "0" is input in the low-order 15 bits of the barrel shifter 204. The number of shifts from the priority encoder 206 is input to the barrel shifter 204, which then selects and outputs arbitrarily consecutive 16-bit data in 31-bit inputs in accordance with the number of shifts. For example, when the number of shifts, 3, is input from the priority encoder 206, the barrel shifter 204 selects inputs N_{27}, N_{26}, N_{25}, ..., N_{12} in the 31-bit inputs, and subsequently outputs the 16-bit data in parallel to outputs S_{15} through S_0.

The 16-bit data output in parallel from the barrel shifter 204 is input to the A-register 202 in parallel and

then held there.

Consequently, the shifting of the number of bits corresponding to the number of shifts from the priority encoder 206 can be performed at one time.

The CT update-logic 211 inputs the number of shifts from the priority encoder 206 and the CT value prior to the re-normalization, and subsequently outputs the number of output bytes and the CT value after the re-normalization.

As shown in Fig. 8, a table representing the correlation between the number of shifts and CT values is provided in the CT update-logic 211. According to the table, the number of output bytes ranges from 0 to 2 when the number of shifts and the CT value range from 1 to 15, and from 1 to 8 respectively. The number of output bytes can be used for control such that an output-control part 210, as shown in Fig. 5, outputs nothing when the output byte number is 0; outputs the code of HIGH register 207 when the output byte number is 1,; and outputs 2 bytes of the HIGH register 207 and the LOW register 208 when the number is 2. Meanwhile, a new CT-value is output from the CT update-logic 211 to the CT-register 205, where the value is held.

In the aforementioned manner, each bit value of a plurality of bits in the A-register is monitored in parallel, and the shift of the plurality of bits in the A-register 202 and the C-register 201 is executed at one time. Accordingly, the match/mismatch between the predictive picture-element data and the target picture-element data to be coded is examined. In addition, period required for the re-normalization can be set to be constant regardless of the contents of the A-register at that time. Therefore, synchronous coding, which can be conducted in real time with the inputting of the target picture-element data to be coded, becomes possible.

The above-mentioned preferred embodiment has been described with regard to a coding circuit using the arithmetic coding device of the subtraction type; however, it is apparent that a decoder can be made by using the equivalent construction to the coding device from the view point of the compatibility between the decoder and the coder of the arithmetic coding device.

Consequently, in the embodiment according to the present invention, the arithmetic coding device can be operable at a constant speed regardless of the re-normalization condition, thus enabling coding or decoding at a high speed.

While the present invention has been described with respect to what is presently considered to be the preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiment. To the contrary, the invention is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

Claims

1. An image coding device for coding image data by using an arithmetic code, comprising:

    examination means (904) for examining coincidence/noncoincidence between actual image data of a target pixel to be coded and predictive image data predicted with reference to image data of reference pixels adjacent to the target pixel;
    first register means (202) for storing a plurality of bits of interval data to be used for coding the image data in accordance with an examination result from said examination means;
    second register means (201) for storing a plurality of bits of code data in accordance with an examination result from said examination means;
    monitor means (206) for monitoring plural bits of the interval data stored in said first register means;
    shift means (203, 204) for shifting the interval data stored in said first register means and the code data stored in said second register means in accordance with a monitoring result from said monitoring means, said shift means being adapted to shift the interval data and the code data by a plurality of bits at one time;
    holding means (205) for holding an amount of shifts of the code data executed by said shift means; and
    output control means (211) for controlling the output of the code data from said second register means in accordance with the amount of shifts being held by said holding means and an amount of shifts of the code data executed by said shift means.

2. An image coding device according to claim 1, wherein said monitor means detects the bit position closest to MSB among all bit positions which store value "1" in said first register means.

3. An image coding device according to claim 2, wherein said shift means shifts the interval data and the code data in accordance with the bit position detected by said monitor means.

4. An image coding device according to claim 2 or 3, wherein said shift means shifts the interval data stored in said first register means so as to move the value "1" stored at the bit position detected by said monitor means to the MSB.

5. An image coding device according to any preceding claim, further comprising updating means for updating the amount of shifts to be held by said holding

means based upon the amount of shifts being held by said holding means and also the amount of shifts of the code data executed by said shift means.

6. An image coding device according to any preceding claim, wherein said output control means controls the amount of the code data to be output from said second register means.

7. An image coding device according to claim 1, wherein said shift means shifts the interval data when the value of the interval data in said first register means is less than a predetermined value.

8. An image coding device according to any preceding claim, further comprising rewriting means for rewriting the interval data in said first register means in accordance with an examination result from said examination means.

9. An image coding method of coding image data by using an arithmetic code, comprising:

an examining step of examining coincidence/noncoincidence between actual image data of a target pixel to be coded and predictive image data predicted with reference to image data of reference pixels adjacent to the target pixel; a first storing step of storing a plurality of bits of interval data to be used for coding the image data in a first register in accordance with an examination result of the examining step; a second storing step of storing a plurality of bits of code data in a second register in accordance with an examination result of the examining step; a monitoring step of monitoring plural bits of the interval data stored in the first register; a shifting step of shifting the interval data stored in the first register and the code data stored in the second register in accordance with a monitoring result of the monitoring step, the interval data and the code data being shifted by a plurality of bits at one time; a holding step of holding an amount of shifts of the code data in the first register; and a controlling step of controlling an output of the code data from the second register in accordance with the amount of shifts being held and an amount of shifts of the code data.

10. An image coding method according to claim 9, wherein in the monitor step, the bit position closest to MSB among all bit positions which store value "1" in the first register is detected.

11. An image coding method according to claim 10, wherein in the shifting step, the interval data and

the code data is shifted in accordance with the detected bit position.

12. An image coding method according to claim 10 or 11, wherein in the shifting step, the interval data stored in the first register is shifted so as to move the value "1" stored at the detected bit position to the MSB.

13. An image coding method according to any of claims 9 to 12, further comprising a step of updating the amount of shifts being held based upon the amount of shifts being held and the amount of shifts of the code data.

14. An image coding method according to any of claims 9 to 13, wherein in the controlling step, the amount of the code data to be output from the second register is controlled.

15. An image coding method according to claim 9, wherein in the shifting step, the interval data is shifted when the value of the interval data in the first register is less than a predetermined value.

16. An image coding method according to any of claims 9 to 15, further comprising a step of rewriting the interval data in the first register in accordance with an examination result of the examining step.

Patentansprüche

1. Bildkodiereinrichtung zur Kodierung von Bilddaten unter Verwendung eines arithmetischen Codes, mit

einer Prüfeinrichtung (904) zur Prüfung der Übereinstimmung/Nicht-Übereinstimmung zwischen tatsächlichen Bilddaten eines zu kodierenden Zielbildelements und Prädiktions-bilddaten, die bezüglich Bilddaten von an das Zielbildelement angrenzenden Bezugsbildelementen vorausgesagt werden, einer ersten Registereinrichtung (202) zur Speicherung einer Vielzahl von Bits von zur Kodierung der Bilddaten zu verwendenden Intervalldaten entsprechend einem Prüfergebnis der Prüfeinrichtung, einer zweiten Registereinrichtung (201) zur Speicherung einer Vielzahl von Bits von Codedaten entsprechend einem Prüfergebnis der Prüfeinrichtung, einer Überwachungseinrichtung (206) zur Überwachung einer Vielzahl von Bits der in der ersten Registereinrichtung gespeicherten Intervalldaten, einer Verschiebungseinrichtung (203, 204) zur Verschiebung der in der ersten Registereinrich-

lung gespeicherten Intervalldaten und der in der zweiten Registereinrichtung gespeicherten Codedaten entsprechend einem Überwachungsergebnis der Überwachungseinrichtung, wobei die Verchiebungseinrichtung zur Verschiebung der Intervalldaten und der Codedaten um eine Vielzahl von Bits zu einem Zeitpunkt eingerichtet ist,
einer Halteeinrichtung (205) zum Halten eines Ausmaßes der durch die Verschiebungseinrichtung ausgeführten Verschiebungen der Codedaten und
einer Ausgabesteuereinrichtung (211) zur Steuerung der Ausgabe der Codedaten aus der zweiten Registereinrichtung entsprechend dem Ausmaß der Verschiebungen, die von der Halteeinrichtung gehalten werden, und einem Ausmaß der durch die Verschiebungseinrichtung ausgeführten Verschiebungen der Codedaten.

2. Bildkodiereinrichtung nach Anspruch 1, wobei die Überwachungseinrichtung die Bitposition erfaßt, die dem höchstwertigen Bit unter allen Bitpositionen am nächsten ist, die den Wert "1" in der ersten Registereinrichtung speichern.

3. Bildkodiereinrichtung nach Anspruch 2, wobei die Verschiebungseinrichtung die Intervalldaten und die Codedaten entsprechend der durch die Überwachungseinrichtung erfaßten Bitposition verschiebt.

4. Bildkodiereinrichtung nach Anspruch 2 oder 3, wobei die Verschiebungseinrichtung die in der ersten Registereinrichtung gespeicherten Intervalldaten verschiebt, um den Wert "1" an das höchstwertige Bit zu bewegen, der an der durch die Überwachungseinrichtung erfaßten Bitposition gespeichert ist.

5. Bildkodiereinrichtung nach einer der vorhergehenden Ansprüche, ferner mit einer Aktualisierungseinrichtung zur Aktualisierung des durch die Halteeinrichtung zu haltenden Ausmaßes der Verschiebungen beruhend auf dem durch die Halteeinrichtung gehaltenen Ausmaß der Verschiebungen und auch auf dem Ausmaß der durch die Verschiebungseinrichtung ausgeführten Verschiebungen der Codedaten.

6. Bildkodiereinrichtung nach einem der vorhergehenden Ansprüche, wobei die Ausgabesteuereinrichtung die aus der zweiten Registereinrichtung auszugebende Menge der Codedaten steuert.

7. Bildkodiereinrichtung nach Anspruch 1, wobei die Verschiebungseinrichtung die Intervalldaten ver-

schiebt, wenn der Wert der Intervalldaten in der ersten Registereinrichtung kleiner als ein vorbestimmter Wert ist.

8. Bildkodiereinrichtung nach einem der vorhergehenden Ansprüche, ferner mit einer Neu-Schreibeinrichtung zum Neu-Schreiben der Intervalldaten in der ersten Registereinrichtung entsprechend einem Prüfergebnis der Prüfeinrichtung.

9. Bildkodierverfahren zur Kodierung von Bilddaten unter Verwendung eines arithmetischen Codes mit

einem Prüfschritt zum Prüfen der Übereinstimmung/Nicht-Übereinstimmung zwischen tatsächlichen Bilddaten eines zu kodierenden Zielbildelements und Prädiktionsbilddaten, die bezüglich Bilddaten von an das Zielbildelement angrenzenden Bezugsbildelementen vorausgesagt werden,
einem ersten Speicherschritt zum Speichern einer Vielzahl von Bits von zur Kodierung der Bilddaten zu verwendenden Intervalldaten in einem ersten Register entsprechend einem Prüfergebnis des Prüfschritts,
einem zweiten Speicherschritt zum Speichern einer Vielzahl von Bits von Codedaten in einem zweiten Register entsprechend einem Prüfergebnis des Prüfschritts,
einem Überwachungsschritt zum Überwachen einer Vielzahl von Bits der in dem ersten Register gespeicherten Intervalldaten,
einem Verschiebungsschritt zum Verschieben der in dem ersten Register gespeicherter Intervalldaten und der in dem zweiten Register gespeicherten Codedaten entsprechend einem Überwachungsergebnis des Überwachungsschritts, wobei die Intervalldaten und die Codedaten um eine Vielzahl von Bits zu einem Zeitpunkt verschoben werden,
einem Halteschritt zum Halten eines Ausmaßes von Verschiebungen der Codedaten in dem ersten Register und
einem Steuerschritt zum Steuern einer Ausgabe der Codedaten aus dem zweiten Register entsprechend dem Ausmaß der Verschiebungen, die gehalten werden, und einem Ausmaß der Verschiebungen der Codedaten.

10. Bildkodierverfahren nach Anspruch 9, wobei in dem Überwachungsschritt die Bitposition erfaßt wird, die dem höchstwertigen Bit unter allen Bitpositionen am nächsten ist, die den Wert "1" in dem ersten Register speichern.

11. Bildkodierverfahren nach Anspruch 10, wobei in dem Verschiebungsschritt die Intervalldaten und die Codedaten entsprechend der erfaßten Bitposi-

tion verschoben werden.

12. Bildkodierverfahren nach Anspruch 10 oder 11, wobei in dem Verschiebungsschritt die in dem ersten Register gespeicherten Intervalldaten verschoben werden, um den an der erfaßten Bitposition gespeicherten Wert "1" an das höchstwertige Bit zu bewegen.

13. Bildkodierverfahren nach einem der Ansprüche 9 bis 12, ferner mit einem Schritt zum Aktualisieren des Ausmaßes der gehaltenen Verschiebungen beruhend auf dem Ausmaß der gehaltenen Verschiebungen und dem Ausmaß der Verschiebungen der Codedaten.

14. Bildkodierverfahren nach einem der Ansprüche 9 bis 13, wobei in dem Steuerschritt die aus dem zweiten Register auszugebende Menge der Codedaten gesteuert wird.

15. Bildkodierverfahren nach Anspruch 9, wobei in dem Verschiebungsschritt die Intervalldaten verschoben werden, wenn der Wert der Intervalldaten in dem ersten Register kleiner als ein vorbestimmter Wert ist.

16. Bildkodierverfahren nach einem der Ansprüche 9 bis 15, ferner mit einem Schritt zum Neu-Schreiben der Intervalldaten in dem ersten Register entsprechend einem Prüfergebnis des Prüfschritts.

Revendications

1. Dispositif de codage d'image destiné à coder des données d'image en utilisant un code arithmétique, comprenant :

   un moyen (904) d'examen destiné à examiner la coïncidence/non-coïncidence entre des données d'image réelles d'un pixel cible à coder et des données d'image prédictives, prédites en se référant à des données d'image de pixels de référence adjacents au pixel cible ;
   un premier moyen (202) formant registre destiné à mémoriser une pluralité de bits de données d'intervalle à utiliser pour coder les données d'image en fonction d'un résultat d'examen provenant dudit moyen d'examen ;
   un second moyen (201) formant registre destiné à mémoriser une pluralité de bits de données de code en fonction d'un résultat d'examen provenant dudit moyen d'examen ;
   un moyen (206) de surveillance destiné à surveiller plusieurs bits de données d'intervalle mémorisées dans ledit premier moyen formant registre ;

   un moyen (203, 204) de décalage destiné à décaler les données d'intervalle, mémorisées dans ledit premier moyen formant registre et les données de code mémorisées dans ledit second moyen formant registre, en fonction d'un résultat de surveillance provenant dudit moyen de surveillance, ledit moyen de décalage étant apte à décaler les données d'intervalle et les données de code d'une pluralité de bits à la fois ;
   un moyen de maintien (205) destiné à maintenir une valeur des décalages des données de code effectués par ledit moyen de décalage ; et
   un moyen (211) de commande de sortie destiné à commander la sortie des données de code dudit second moyen formant registre en fonction de la valeur des décalages qui sont maintenus par ledit moyen de maintien et d'une valeur des décalages des données de code effectués par ledit moyen de décalage.

2. Dispositif de codage d'image selon la revendication 1, dans lequel ledit moyen de surveillance détecte la position de bit la plus proche du bit de poids fort parmi toutes les positions de bit qui mémorisent la valeur "1" dans ledit premier moyen formant registre.

3. Dispositif de codage d'image selon la revendication 2, dans lequel ledit moyen de décalage décale les données d'intervalle et les données de code en fonction de la position de bit détectée par ledit moyen de surveillance.

4. Dispositif de codage d'image selon la revendication 2 ou 3, dans lequel ledit moyen de décalage décale les données d'intervalle mémorisées dans ledit premier moyen formant registre de façon à amener, au bit de poids fort, la valeur "1" mémorisée à la position de bit détectée par ledit moyen de surveillance.

5. Dispositif de codage d'image selon l'une quelconque des revendications précédentes, comprenant en outre un moyen de mise à jour destiné à mettre à jour la valeur des décalages à maintenir par ledit moyen de maintien en se basant sur la valeur des décalages qui sont maintenus par ledit moyen de maintien et aussi sur la valeur des décalages des données de code effectués par ledit moyen de décalage.

6. Dispositif de codage d'image selon l'une quelconque des revendications précédentes, dans lequel ledit moyen de commande de sortie commande la valeur des données de code à sortir dudit second moyen formant registre.

7. Dispositif de codage d'image selon la revendication

1, dans lequel ledit moyen de décalage décale les données d'intervalle lorsque la valeur des données d'intervalle dans ledit premier moyen formant registre est plus petite qu'une valeur prédéterminée.

8. Dispositif de codage d'image selon l'une quelconque des revendications précédentes, comprenant en outre un moyen de réécriture destiné à réécrire les données d'intervalle dans ledit premier moyen formant registre en fonction d'un résultat d'examen provenant dudit moyen d'examen.

9. Procédé de codage d'image destiné à coder des données d'image en utilisant un code arithmétique comprenant :

une étape d'examen destinée à examiner la coïncidence/non-coïncidence entre des données d'image réelles d'un pixel cible à coder et des données d'image prédictives, prédites en se référant à des données d'image de pixels de référence adjacents au pixel cible ;
une première étape de mémorisation destinée à mémoriser une pluralité de bits de données d'intervalle à utiliser pour coder les données d'image dans un premier registre en fonction d'un résultat d'examen de l'étape d'examen ;
une seconde étape de mémorisation destinée à mémoriser une pluralité de bits de données de code dans un second registre en fonction d'un résultat d'examen de l'étape d'examen ;
une étape de surveillance destinée à surveiller plusieurs bits des données d'intervalle mémorisées dans le premier registre ;
une étape de décalage destinée à décaler les données d'intervalle mémorisées dans le premier registre et les données de code mémorisées dans le second registre en fonction d'un résultat de surveillance de l'étape de surveillance, les données d'intervalle et les données de code étant décalées d'une pluralité de bits à la fois ;
une étape de maintien destinée à maintenir une valeur des décalages des données de code dans le premier registre; et
une étape de commande destinée à commander une sortie des données de code du second registre en fonction de la valeur des décalages qui sont maintenus et d'une valeur des décalages des données de code.

10. Procédé de codage d'image selon la revendication 9, dans lequel, dans l'étape de surveillance, on détecte la position de bit la plus proche du bit de poids fort parmi toutes les positions de bit qui mémorisent la valeur "1" dans le premier registre.

11. Procédé de codage d'image selon la revendication

10, dans lequel, dans l'étape de décalage, on décale les données d'intervalle et les données de code en fonction de la position de bit détectée.

12. Procédé de codage d'image selon la revendication 10 ou 11, dans lequel, dans l'étape de décalage, on décale les données d'intervalle mémorisées dans le premier registre de façon à amener, au bit de poids fort, la valeur "1" mémorisée à la position de bit détectée.

13. Procédé de codage d'image selon l'une quelconque des revendications 9 à 12, comprenant en outre une étape de mise à jour de la valeur des décalages à maintenir, en se basant sur la valeur de décalages qui sont maintenus et sur la valeur des décalages des données de code.

14. Procédé de codage d'image selon l'une quelconque des revendications 9 à 13, dans lequel, dans l'étape de commande, on commande la valeur des données de code à sortir du second registre.

15. Procédé de codage d'image selon la revendication 9, dans lequel, dans l'étape de décalage, on décale les données d'intervalle lorsque la valeur des données d'intervalle dans le premier registre est plus petite qu'une valeur prédéterminée.

16. Procédé de codage d'image selon l'une quelconque des revendications 9 à 15, comprenant en outre une étape de réécriture des données d'intervalle dans le premier registre en fonction d'un résultat d'examen de l'étape d'examen.
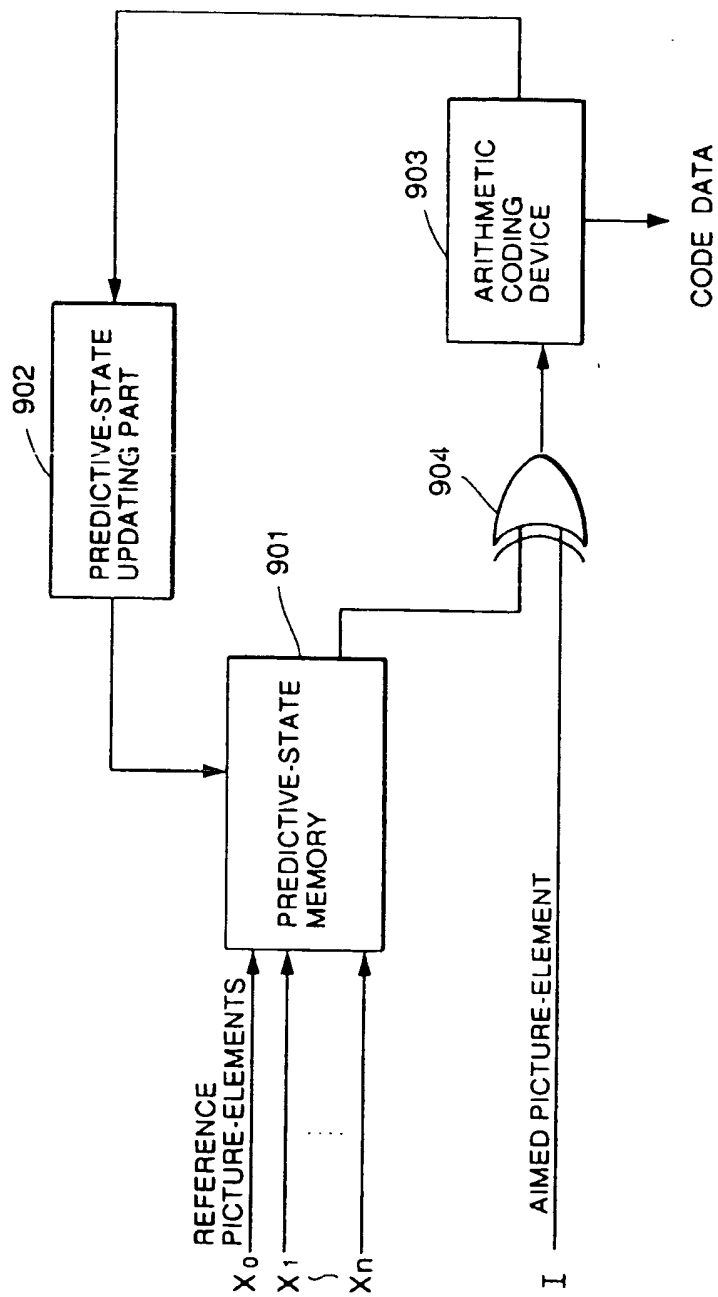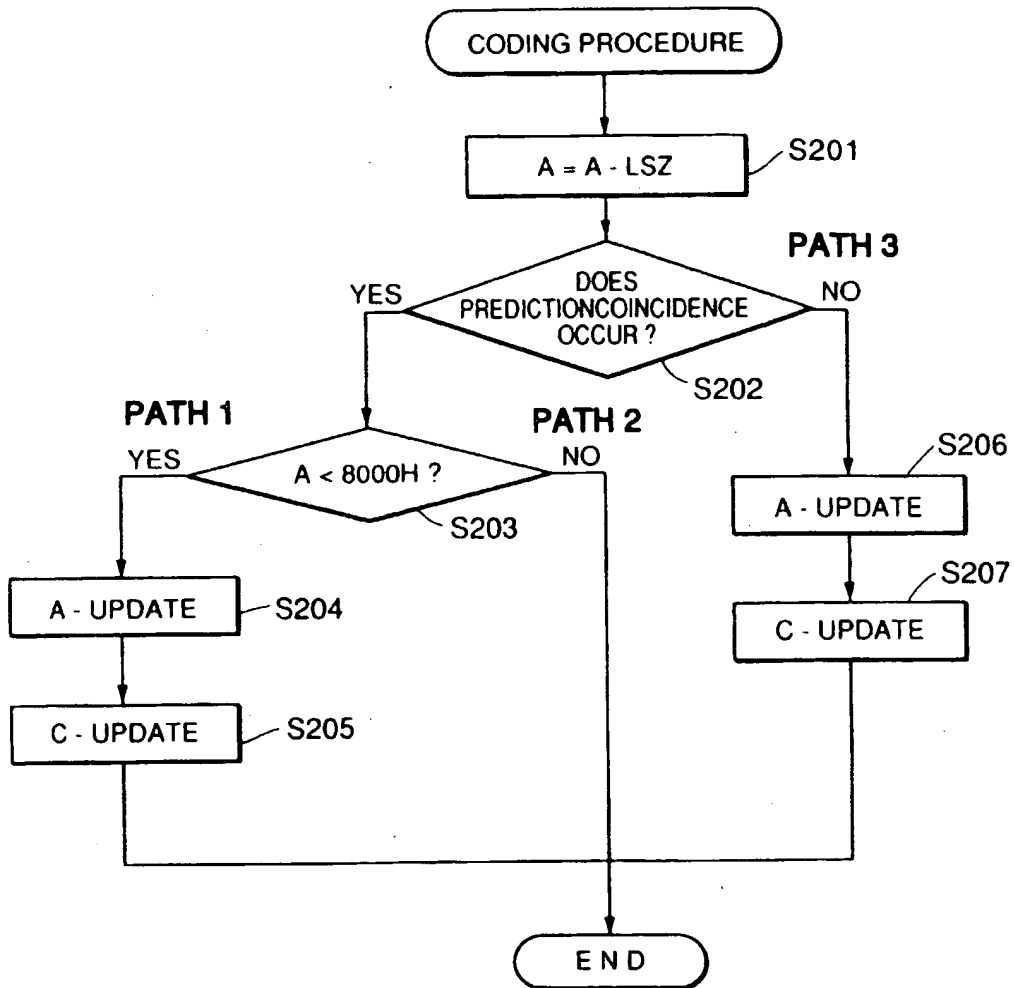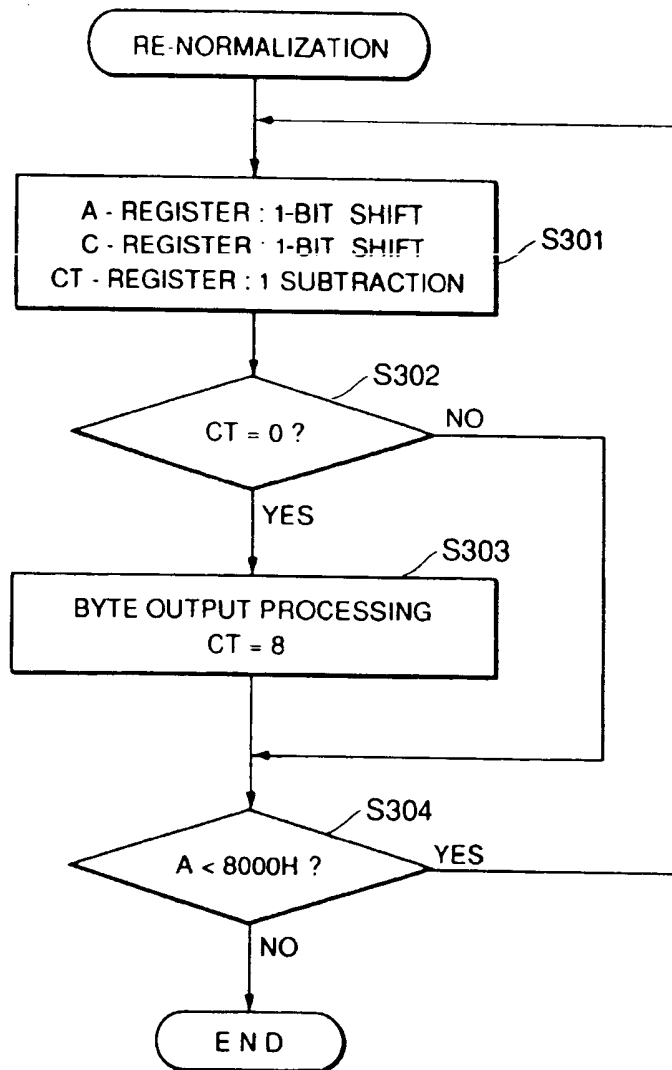
FIG. 1

FIG. 2A

FIG. 2B

```
        ┌──────────────────────┐
        │  RE-NORMALIZATION     │
        └──────────────────────┘
                   │
        ┌──────────────────────┐
        │ A - REGISTER : 1-BIT  SHIFT     │
        │ C - REGISTER : 1-BIT  SHIFT     │ ── S301
        │ CT - REGISTER : 1 SUBTRACTION   │
        └──────────────────────┘
                   │
                  ╱╲  S302
                 ╱  ╲        NO
                ╱ CT = 0 ? ╲─────────┐
                ╲          ╱          │
                 ╲        ╱           │
                  ╲╱                  │
                   │ YES              │
        ┌──────────────────────┐     │
        │ BYTE OUTPUT PROCESSING │ ── S303
        │ CT = 8                 │     │
        └──────────────────────┘     │
                   │                  │
                   ├──────────────────┘
                   │
                  ╱╲  S304
                 ╱  ╲        YES
                ╱ A < 8000H ?╲────────┐ (loop back to S301)
                ╲          ╱          
                 ╲        ╱           
                  ╲╱                  
                   │ NO               
        ┌──────────────────────┐
        │        E N D          │
        └──────────────────────┘
```

FIG. 3

FIG. 4

FIG. 5

FIG. 6

TO CT-UPDATE
211 AND
BARREL SHIFTERS
203 AND 204
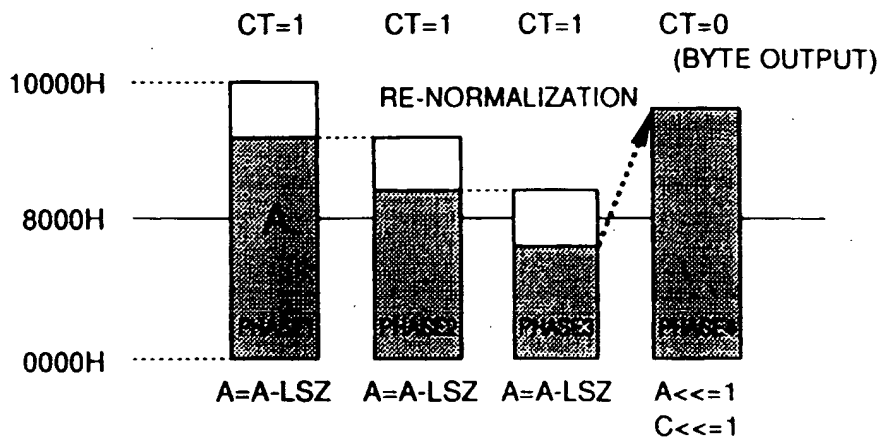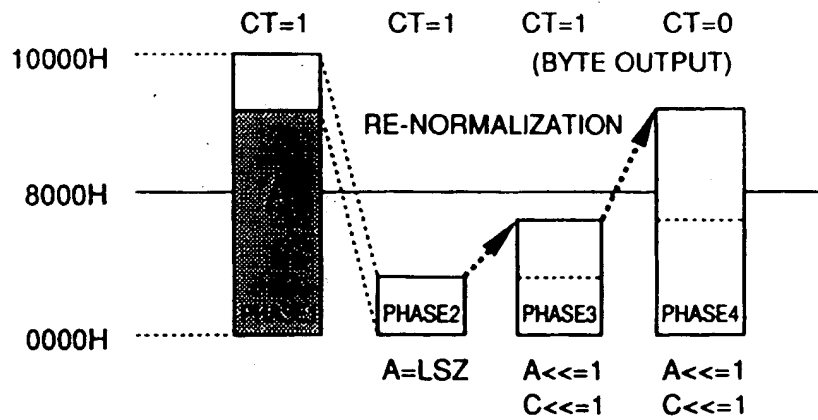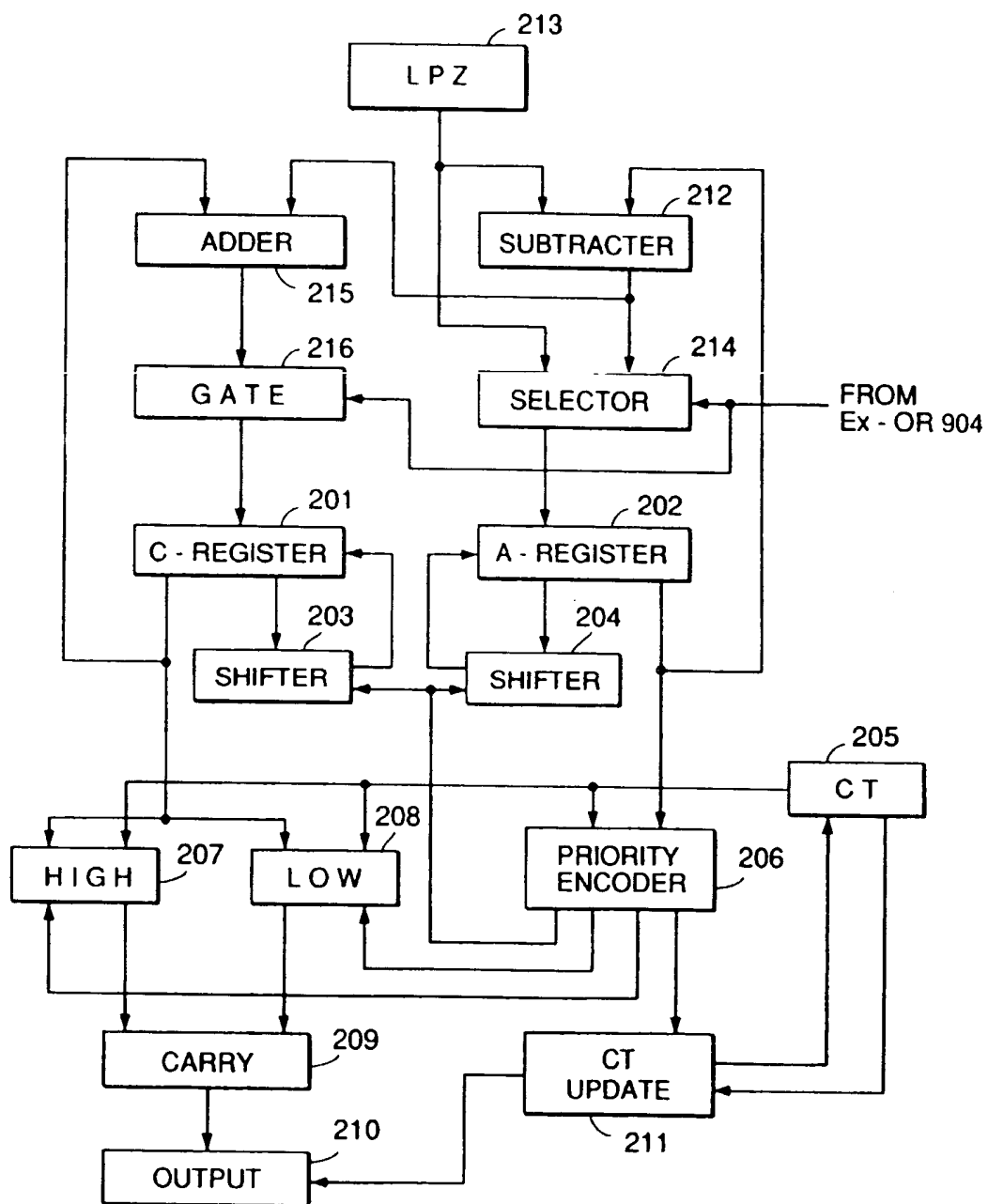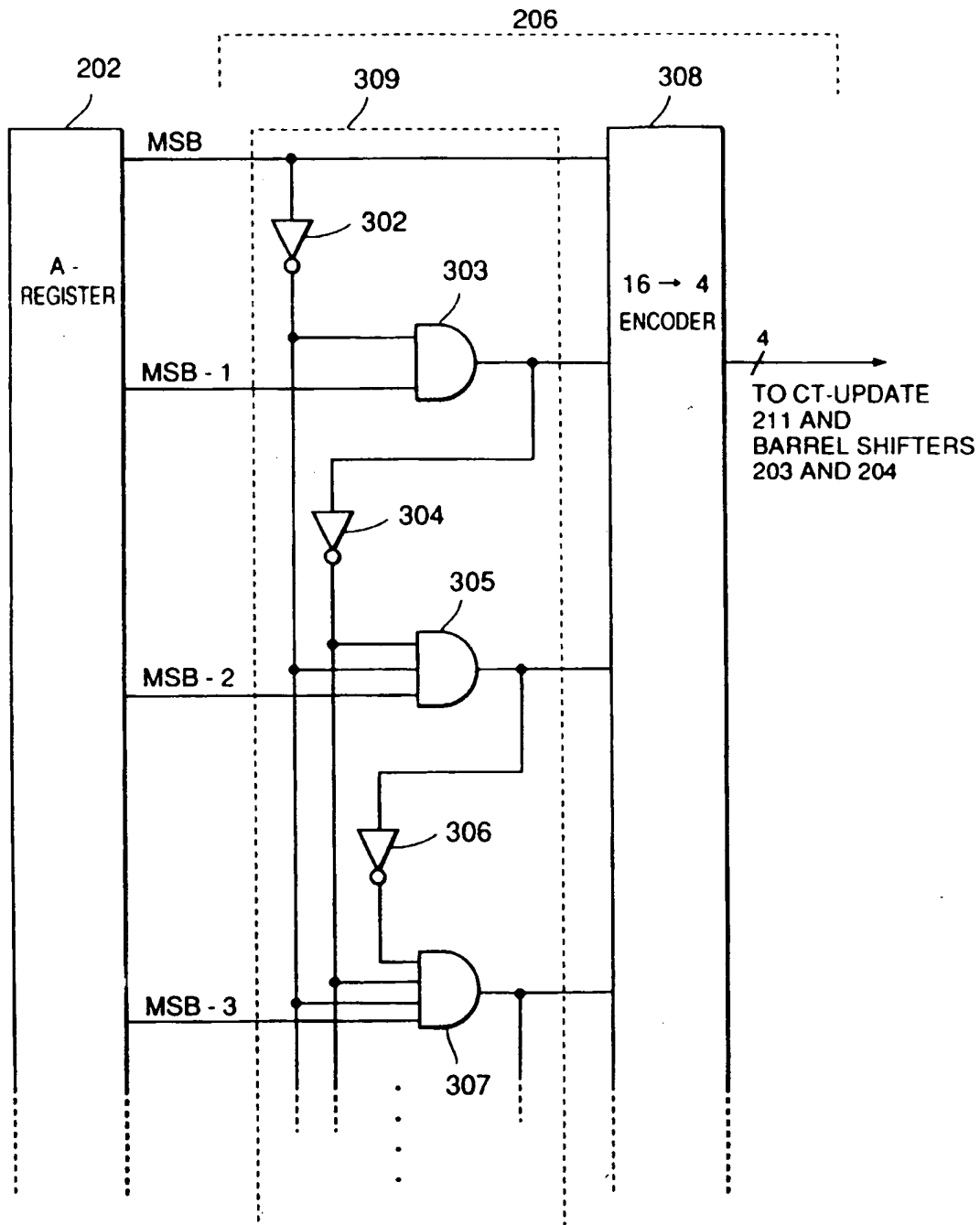
FIG. 7

RANGES OF A	THE NUMBER OF SHIFTS
1	15
2 ~ 3	14
4 ~ 7	13
8 ~ FH	12
10H ~ 1 FH	11
20H ~ 3 FH	10
40H ~ 7 FH	9
80H ~ FFH	8
100H ~ 1FFH	7
200H ~ 3FFH	6
400H ~ 7FFH	5
800H ~ FFFH	4
1000H ~ 1 FFFH	3
2000H ~ 3 FFFH	2
4000H ~ 7 FFFH	1

FIG. 8

CT VALUE PRIOR TO RE-NORMALIZATION

THE NUMBER OF SHIFTS

	1	2	3	4	5	6	7	8
1	1 / 8	0 / 1	0 / 2	0 / 3	0 / 4	0 / 5	0 / 6	0 / 7
2	1 / 7	1 / 8	0 / 1	0 / 2	0 / 3	0 / 4	0 / 5	0 / 6
3	1 / 6	1 / 7	1 / 8	0 / 1	0 / 2	0 / 3	0 / 4	0 / 5
4	1 / 5	1 / 6	1 / 7	1 / 8	0 / 1	0 / 2	0 / 3	0 / 4
5	1 / 4	1 / 5	1 / 6	1 / 7	1 / 8	0 / 1	0 / 2	0 / 3
6	1 / 3	1 / 4	1 / 5	1 / 6	1 / 7	1 / 8	0 / 1	0 / 2
7	1 / 2	1 / 3	1 / 4	1 / 5	1 / 6	1 / 7	1 / 8	0 / 1
8	1 / 1	1 / 2	1 / 3	1 / 4	1 / 5	1 / 6	1 / 7	1 / 8
9	2 / 8	1 / 1	1 / 2	1 / 3	1 / 4	1 / 5	1 / 6	1 / 7
10	2 / 7	2 / 8	1 / 1	1 / 2	1 / 3	1 / 4	1 / 5	1 / 6
11	2 / 6	2 / 7	2 / 8	1 / 1	1 / 2	1 / 3	1 / 4	1 / 5
12	2 / 5	2 / 6	2 / 7	2 / 8	1 / 1	1 / 2	1 / 3	1 / 4
13	2 / 4	2 / 5	2 / 6	2 / 7	2 / 8	1 / 1	1 / 2	1 / 3
14	2 / 3	2 / 4	2 / 5	2 / 6	2 / 7	2 / 8	1 / 1	1 / 2
15	2 / 2	2 / 3	2 / 4	2 / 5	2 / 6	2 / 7	2 / 8	1 / 1

Legend: THE NUMBER OF OUTPUT BYTES / NEW CT VALUE

FIG. 9